Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N/C**
2. **– IN**
3. **+ IN**
4. **V –**
5. **N/C**
6. **OUT**
7. **V +**
8. **N/C**

**.098”**

**.073”**

**117H**



**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 117H**

**APPROVED BY: DK DIE SIZE .073” X .098” DATE: 1/22/16**

**MFG: LINEAR TECH THICKNESS .025” P/N: LM117**

**DG 10.1.2**

#### Rev B, 7/1